We claim:

1 (previously presented). A monolithically integrated vertical PIN photodiode formed in biCMOS technology and having a substantially planar surface facing the light and having a back side and anode terminals via p regions on a topside of the photodiode, wherein an i-zone of the PIN photodiode is formed by:

(a) a combination of a first p^- epitaxial layer with a thickness of substantially 15µm at most and having a dopant concentration of less than $5 * 10^{14}$ cm^{-3}, wherein the p^- epitaxial layer is located on a p substrate;

(b) a slightly doped n^- epitaxial layer adjacent to the first layer and having a dopant concentration in a range of substantially 10^{14} cm^{-3} to 10^{15} cm^{-3}, wherein the n^+ cathode of the PIN photodiode is incorporated into the second layer; and

wherein, in lateral direction, p regions delineate the second n epitaxial layer, and in addition to the anode terminals, a further anode contact area of the PIN diode is provided at the back side.

2 (previously presented). The PIN photodiode of claim 1, wherein buried p^+ layers extending into the p epitaxial layer are located below the p regions which border the second n epitaxial layer in the lateral direction.

3 (previously presented). The PIN photodiode of claim 1, wherein at least within the further anode contact area, acting as a back side, a silicon wafer bearing the photodiode is thinned.

4 (previously presented). The PIN photodiode of claim 1 wherein the anode of the PIN photodiode is electrically contacted from the frontside only.

5 (original). The PIN photodiode of claim 4, wherein one or more anode terminals are formed by deep trench contacts.

6 (previously presented). The PIN photodiode of claim 1, wherein the slightly doped n^- epitaxial layer has a dopant concentration of approximately 10^{14} cm^{-3}.

7 (previously presented). The PIN photodiode of claim 1, wherein the dopant concentration of the first epitaxial layer is substantially 10^{+13} cm^{-3}.

8 (previously presented) The PIN photodiode of claim 1, wherein the p regions are configured as p wells in a vertical section.

9 (previously presented) The PIN photodiode of claim 8, wherein the wells extend to the first.

10 (previously presented). The PIN photodiode of claim 1, wherein a dopant concentration of the second layer is less than a dopant concentration of an n region in the second layer, wherein the n region forms the collector doping for contacting a cathode.

11 (previously presented). The PIN photodiode of claim 1, wherein within and spaced apart from the p regions, a cathode region is provided.

12(withdrawn). A method for forming a monolithically integrated vertical PIN photodiode according to a biCMOS technology, wherein:

(i) a p^+ silicon wafer having a p^- epitaxial layer with a maximum thickness of substantially 15µm and having a dopant concentration of approximately 10^{13} cm^{-3} is used as base material;

(ii) after a subsequent implementation of a buried layer a following n epitaxial layer having a dopant concentration within a range of approximately 10^{14} cm^{-3} is one of deposited and incorporated; and

(iii) thereafter, n and p wells are formed and standard following process steps of the technology are performed, wherein in the n^- epitaxial layer an n^+ cathode of the PIN photodiode is incorporated, and in a lateral direction p regions delineate the n epitaxial layer and wherein in addition to anode terminals via the p regions of the planar topside a further anode contact area is formed on the back side.

13 (withdrawn). The method of claim 12, wherein finally the silicon wafer at least within the area of the PIN diode is thinned at the back side with a protective covering formed on the front side.

14 (withdrawn). The method of claim 12, wherein the anode contact area of the back side is not particularly formed and is not electrically contacted.

15 (withdrawn). The method of claim 12, wherein the back side anode of a chip provided after dicing of the substrate can electrically be contacted by attaching the chip to a lead frame or a conductive area of a wiring board by means of a conductive adhesive, if the serial resistance is not sufficient.

16 (previously presented). A monolithically vertical PIN photodiode formed in biCMOS technology, wherein an i-zone of the PIN diode is formed by the combination of a slightly doped p^- epitaxial layer having a thickness up to substantially 15µm with a dopant concentration of less than $5 * 10^{14}$ cm^{-3} and being located on a highly doped p^+ substrate, with a slightly doped n^- epitaxial layer formed adjacent to the p^- epitaxial layer and having a dopant concentration in the range of approximately 10^{14} cm^{-3} , as range of dopant concentration $\leq 10^{14}$ cm^{-3} to $< 10^{15}$ cm^{-3}, into which the n^+ cathode of the PIN photodiode is incorporated, wherein p regions laterally delineate the n epitaxial

layer in lateral direction and wherein in addition to the anode terminals a further anode contact area of the PIN diode is provided at the back side via the p well regions of the planar front side.

17 (previously presented). The monolithically integrated vertical PIN photodiode of claim 16, wherein the range of dopant concentration is substantially 10^{13} cm^{-3}.

18 (original). The monolithically integrated vertical PIN photodiode of claim 16, characterized in that buried p^+ layers extending into the p epitaxial layer are located below the p regions, which laterally delineate the n epitaxial layer in lateral direction.

19 (original). The monolithically integrated vertical PIN photodiode of claim 16, characterized in that at least within the back side anode, the silicon wafer is thinned.

20 (original). The monolithically integrated vertical PIN photodiode of claim 16, characterized in that the anode of the PIN photodiode is electrically contacted from the front side only.

21 (original). The monolithically integrated vertical PIN photodiode of claim 20, wherein one or more anode terminals are formed by deep trench contacts.

22 (withdrawn) A method of forming a monolithically integrated vertical PIN photodiode in biCMOS technology, wherein:

(i) a p^+ silicon wafer having formed thereon a p^- epitaxial layer with a thickness of approximately 15µm and having a dopant concentration of approximately 10^{13} cm^{-3} is used as an initial material;

(ii) after the subsequent implementation of the buried layer, the n epitaxial layer subsequently formed according to a standard process flow is deposited with a dopant concentration having about 10^{14} cm^{-3}; and

(iii) thereafter, the n and p wells are formed and all further standard subsequent process steps of the technology are performed, wherein the n^+ cathode of the PIN photodiode is incorporated into the n^- epitaxial layer, wherein in lateral direction p regions laterally delineate the n epitaxial layer and wherein in addition to anode terminals, a further anode contact area of the PIN diode is formed on the back side via the p well regions of the planar front side such that said further anode contact area of the chip obtained after the dicing of the substrate can be contacted by attaching the chip to a lead frame or a conductive area of a wiring board by means of a conductive adhesive, to support a sufficiently small serial resistance.

23 (withdrawn). The method of claim 22, wherein in that in a final step the silicon wafer is thinned at the back side at least within the PIN diode with the front side being covered by a protective covering.

24 (withdrawn). The method of claim 22, wherein the anode contact area on the back side not particularly being formed and not electrically being contacted.

25 (previously presented). The PIN photodiode of claim 1, wherein the p^- epitaxial layer is located on a highly doped p substrate.

26 (previously presented). The PIN photodiode of claim 2, wherein the p regions are configured as p wells in a vertical section and wherein the p wells extend to the buried layer.